ated that the distances d_1 & d_2 are typically selected to be sufficiently large in order to eliminate gate oxide weakness in the rounded portion of the layout while maintaining adequate distance of gate members **18***a* & **18***b* from the respective field plates (not shown) disposed in dielectric regions **15***a* & **15***b*. Electrical contact of the rounded fingertip portion of gate members **18***a* & **18***b* to the gate metal trace/bus may be made as shown in FIG. **10** or FIG. **11**.

Although the above embodiments have been described in conjunction with a specific device types, those of ordinary skill in the arts will appreciate that numerous modifications and alterations are well within the scope of the present invention. For instance, although HVFETs have been described, the methods, layouts and structures shown are equally applicable to other structures and device types, including Schottky, diode, IGBT and bipolar structures. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

We claim:

1. A transistor comprising:

a pillar of semiconductor material arranged in a racetrack-shaped layout having a substantially linear section that extends in a first lateral direction and rounded sections at each end of the substantially linear section of the racetrack-shaped layout, a source region of a first conductivity type being disposed at or near a top surface of the pillar, and a body region of a second conductivity type being disposed in the pillar beneath the source region;

first and second dielectric regions disposed on opposite sides of the pillar, respectively, the first dielectric region being laterally surrounded by the pillar, and the second dielectric region laterally surrounding the pillar;

first and second field plates respectively disposed in the first and second dielectric regions;

first and second gate members respectively disposed in the first and second dielectric regions at or near the top surface of the pillar adjacent the body region, the first and second gate members being separated from the body region by a gate oxide having a first thickness in the substantially linear section of the racetrack-shaped layout, the gate oxide having a second thickness at the rounded sections, the second thickness being substantially larger than the first thickness.

2. The transistor of claim **1** wherein the first thickness is approximately 500 Å.

3. The transistor of claim **1** wherein the second thickness is approximately 1 μm.

4. The transistor of claim **1** further comprising an extended drain region disposed in the pillar beneath the body region.

5. The transistor of claim **1** wherein a length of the substantially linear section in the first lateral direction is at least 30 times greater than a width of the racetrack-shaped layout, the width being in a second lateral direction orthogonal to the first lateral direction.

6. The transistor of claim **1** wherein the first and second gate members are completely insulated from the first and second field plates.

7. A transistor comprising:

a pillar of semiconductor material arranged in a racetrack-shaped layout having a substantially linear section that extends in a first lateral direction and rounded sections at each end of the substantially linear section of the racetrack-shaped layout;

first and second dielectric regions disposed on opposite sides of the pillar, respectively, the first dielectric region being laterally surrounded by the pillar, and the second dielectric region laterally surrounding the pillar;

first and second field plates respectively disposed in the first and second dielectric regions;

first and second gate members respectively disposed in the first and second dielectric regions at or near a top of the pillar, the first and second gate members being separated from the body region by a gate oxide having a first thickness in the substantially linear section of the racetrack-shaped layout, the gate oxide having a second thickness at the rounded sections, the second thickness being substantially larger than the first thickness.

8. The transistor of claim **7** wherein the first thickness is approximately 500 Å.

9. The transistor of claim **7** wherein the second thickness is approximately 1 μm.

10. The transistor of claim **7** further comprising:

a body region disposed in the pillar beneath the source region; and

an extended drain region disposed in the pillar beneath the body region.

11. The transistor of claim **7** wherein a length of the substantially linear section in the first lateral direction is at least 30 times greater than a width of the racetrack-shaped layout, the width being a second lateral direction orthogonal to the first lateral direction.

12. A transistor comprising:

a racetrack-shaped pillar of semiconductor material having spaced-apart first and second linear portions that each extend in a first lateral direction, a first rounded portion of the racetrack-shaped pillar joining respective first ends of the first and second linear portions, a second rounded portion of the racetrack-shaped pillar joining respective second ends of the first and second linear portions;

first and second dielectric regions respectively disposed on opposite sides of the racetrack-shaped pillar, the first dielectric region being laterally surrounded by the pillar, and the second dielectric region laterally surrounding the pillar;

first and second field plates respectively disposed in the first and second dielectric regions;

first and second gate members respectively disposed in the first and second dielectric regions at or near a top of the first linear portion of the racetrack-shaped pillar;

third and fourth gate members respectively disposed in the first and second dielectric regions at or near a top of the second linear portion of the racetrack-shaped pillar; and

wherein the first, second, third and fourth gate members are each separated from the racetrack-shaped pillar by a gate oxide, opposite ends of the first, second, third and fourth gate members being terminated in the first lateral direction at or near the first and second rounded portions, respectively.

13. The transistor of claim **12** wherein the first, second, third and fourth gate members each comprise polysilicon.

14. The transistor of claim **12** wherein the gate oxide is approximately 500 Å thick.

15. The transistor of claim **12** wherein a length of the substantially linear portion in the first lateral direction is at least 30 times greater than a distance separating the first and second substantially linear portions in a second lateral direction orthogonal to the first lateral direction.

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